Selective Epitaxial Growth of Silicon for Vertical Diode Application

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Received September 28, 2009; revised November 30, 2009; accepted December 4, 2009; published online August 20, 2010

Abstract

Selective epitaxial growth (SEG) has been intensively studied, and many studies have explored numerous growth techniques such as plasma enhanced chemical vapor deposition (PECVD), ultrahigh vacuum CVD (UHV-CVD), and UHV rapid thermal-CVD (UHV-RTCVD). Recently, SEG has extended its versatility to silicon-on-insulator (SOI) devices and cell switches for next generation memories, including device isolation, epitaxial lateral overgrowth (ELO), and elevated source/drain (ESD) fabrication for the metal oxide semiconductor field effect transistor (MOSFET) structure. Silicon or SiGe has been intensively studied, and many studies have explored numerous growth techniques such as plasma enhanced chemical vapor deposition (PECVD), ultrahigh vacuum CVD (UHV-CVD), and UHV rapid thermal-CVD (UHV-RTCVD). Recently, SEG has extended its versatility to novel technologies. Jung et al. have reported the fabrication of a high density static random access memory (SRAM) using the Si-SEG technique for stacking silicon layers.

In this study, we investigate the practical and quantitative selectivity characteristics of Si-SEG in deep contact patterns with that of polycrystalline silicon (poly-Si). The control of selectivity loss during the SEG process is the most crucial for accomplishing process performance since the material and device properties, including crystallinity and electrical characteristics, show marked deviations from the desired results. Unfortunately, the selectivity window of the SEG process has been determined using blanket wafers, so that it was impossible to predict the practical window of real patterned wafers.

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2. Experimental Procedure

200 mm and p-type Si(100) wafers were used as substrates and shallow trench isolation (STI) was carried out. An active area was heavily doped with phosphorus and arsenic. After the deposition of the etch-stop layer, two types of mold layers were prepared. A single-mold structure consists of only CVD SiO₂, whereas the triple-mold structure consists of a CVD SiO₂/low-pressure CVD (LPCVD) SiNₓ/CVD SiO₂ stack. The total thickness of the mold layers was maintained to be 600 nm. The contact holes were patterned using the conventional photolithography and reactive ion etching (RIE) processes. The LPCVD reactor with the SiH₄/dichlorosilane (DCS)/HCl gas system, which has been the most commonly used gas system among those used in the SEG processes, was introduced to grow a Si-SEG layer within the contacts. Poly-Si was also deposited to fill contact holes in some samples. The deposition conditions of Si-SEG and poly-Si are listed in Table I. Selectivity loss was counted for the samples with Si-SEG immediately after the growth of the silicon layer and after the separation of the silicon nodes. A commercialized inspection tool (Tencor KLA2351) with optical source signals (wavelength, 400–600 nm) was introduced to investigate the patterned area of 200 mm wafers and quantify the selectivity loss in the contact holes. The tool detects the abnormalities of repetitive patterns and classifies them as defects. It compares output signals of cells on the wafers. When selectivity losses occur in deep contact patterns, the output signals of abnormal cells are different from those of normal cells, and the tool counts them as defects. The addresses of abnormalities were sampled, and then they were reviewed by scanning electron microscopy (SEM) for the quantification of selectivity loss. Boron was implanted to form a pn diode, and metallization was carried out to measure the electrical properties of the diode with poly-Si and Si-SEG.

3. Results and Discussion

It is crucial to measure and define absolute values of selectivity loss in real contact patterns because the loss in selectivity can affect the crystallinity of the SEG as well as

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1. Introduction

For several decades, the selective epitaxial growth (SEG) technique has attracted world-wide attention for its applications to silicon devices, including device isolation, epitaxial lateral overgrowth (ELO), and elevated source/drain (ESD) fabrication for the metal oxide semiconductor field effect transistor (MOSFET) structure. Silicon or SiGe has been intensively studied, and many studies have explored numerous growth techniques such as plasma enhanced chemical vapor deposition (PECVD), ultrahigh vacuum CVD (UHV-CVD), and UHV rapid thermal-CVD (UHV-RTCVD). Recently, SEG has extended its versatility to novel technologies. Jung et al. have reported the fabrication of a high density static random access memory (SRAM) using the Si-SEG technique for stacking silicon layers.

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Table I. Deposition conditions of Si-SEG and poly-Si layer.

<table>
<thead>
<tr>
<th>Diode material</th>
<th>Gas</th>
<th>Temperature (°C)</th>
<th>Pressure (Torr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si-SEG</td>
<td>H₂/DCS/HCl</td>
<td>800</td>
<td>0.5</td>
</tr>
<tr>
<td>Poly-Si</td>
<td>SiH₄</td>
<td>620</td>
<td>0.5</td>
</tr>
</tbody>
</table>

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circuit operation. If selectivity losses occur during the SEG process, that is, if stable silicon nuclei are formed along the contact sidewall or on top of the oxide window, then they will tend to spontaneously grow and polycrystalline silicon will be formed due to the high temperature (>700°C) of the SEG process. Figure 1 shows a SEM image of a real selectivity loss in contact patterns. Once silicon islands block contact holes, they prevent the further supply of the process gasses into the contacts, and finally vacancies are left within the contacts. Commercialized inspection tool with optical source signals turned out to distinguish selectivity losses. Figure 2 shows a typical map of defects detected by the tool. All the dots represent abnormalities and potential possibilities of selectivity loss. After reviewing dots of abnormalities by SEM, more than 80% of defects were identified by SEM. Figure 3(a) shows an example of a defect address in a triple mold structure after separating the silicon nodes. The contacts that are classified as defects have darker contrast on SEM images than those classified as normal, implying that the contacts are electrically open owing to vacancies within them, so that more electrons are charged-up at defective contacts. Transmission electron microscopy (TEM) analysis reveals that an epitaxially grown silicon layer with crystalline facet is observed at the bottom of the contact, whereas the poly-Si roof is on top, and the subsequent vacancy is in the middle of the contact, as is shown in Fig. 3(b). The selectivity loss in Si-SEG induces the degradation of electrical mobility in the channel silicon layer when it is applied to the channel layers in stacked devices due to the lack of a single crystalline silicon source. Furthermore, no current flows through the vertical switches in the application to next generation memories, which manifest themselves to be failed in device operation.

Practical quantification was conducted with respect to the mold structures and process conditions. As the process time of the SEG or the growth height increases from 200 to 600 nm, the number of defective contacts increases, as is shown in Fig. 4. The average height of SEG was measured from the top of the silicon substrate within contact patterns. The HCl/(DCS + HCl) ratio was maintained to be 0.33. It is difficult to avoid selectivity loss when the SEG process time is increased since the possibility to form stable silicon nuclei increases. Figure 4 also shows the dependence of practical
selectivity on the contact mold material in which single-mold oxide consists of LP-CVD oxide only, while triple-mold oxide consists of LP-CVD SiO$_2$/SiN$_x$/SiO$_2$ sandwich layers. It is obvious that the insertion of the SiN$_x$ layer deteriorates selectivity during the SEG process. Selectivity loss was observed to increase at 600 nm in the single-mold structure. However, the triple-mold structure showed a noticeable increase at 400 nm and a further increase at 600 nm. Claassen and Bloem reported silicon saturation nucleation density ($N_s$) as a function of carrier gas (H$_2$–N$_2$) concentration and oxide-nitride field material at 1000 °C. They showed that the nucleation density of nitride is always larger than that of oxide regardless of the carrier gas concentration [$P_{H_2}/(P_{H_2} + P_{N_2})$], which is consistent with the results shown in Fig. 4.

Although integration parameters including contact etching and wet-cleaning chemistry as well as oxide material were also closely associated with selectivity loss, which is not dealt with in this paper, the most effective method to suppress the generation of defects is to increase the HCl amount during the SEG process as shown in Fig. 5. The average height of SEG was maintained to be 600 nm. As the HCl/(DCS + HCl) ratio increases from 0.33 to 0.52, the number of defects exponentially decreases regardless of mold oxide structures, and finally the defects fewer than 100 in the whole wafer are obtained at HCl/(DCS + HCl) = 0.41.

The electrical properties of the vertical pn diode that is made of Si-SEG and with poly-Si were examined and summarized in Table II. The forward bias characteristics of the vertical pn diode that is made of selectively grown silicon is shown in Fig. 6. The rate of current increase in the minority carrier diffusion-current region (0.65 < $V$ ≤ 0.85) was 69 mV/decade for the SEG diodes, which is comparable to that of the ideal silicon diode (59.5 mV/decade). On the other hand, the conventional poly-Si diodes show a rate of 89 mV/decade. The ideality factors for the SEG diode and the poly-Si diode, which were extracted from the same voltage range, were 1.15 and 1.50, respectively. As for the Si-SEG diode, the deviations of the ideality factor and the swing from those of the ideal diode are believed to be due to the stacking faults in the Si-SEG layer and the dangling bonds in Si/SiO$_2$ around the mold oxide layer. The poly-Si diode contains grain boundaries as well as crystallographic defects within grains. It is reasonable that these imperfections act as generation-recombination centers that disturb current flow. The reverse leakage current of the pn diode was measured at −3 V. The diode with Si-SEG shows a lower leakage current than that with poly-Si by one order of magnitude.

4. Conclusions
We studied the practical selectivity of applying Si-SEG in deep contact patterns to stacked devices and to next-generation memories. The Commercialized in-line tool was successfully used for detecting and quantifying the real number of selectivity loss in 200 mm wafers with real contact patterns. We investigated the average height of Si-
SEG, the structure of mold oxide, and the gas ratio during the SEG process to estimate the efficiency of the proposed method. HCl/(DCS + HCl) ratio was proven to be the most crucial parameter for decreasing selectivity loss. The vertical diode of Si-SEG, with careful selectivity control, showed superior electrical properties to those of the poly-Si. An ideal factor of 1.15 and a reverse leakage current of $3.7 \times 10^{-13}$ A were obtained when using the Si-SEG diode, and it was confirmed that Si-SEG is a suitable material for higher on-current driving diodes than conventional poly-Si.

Acknowledgment

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2009-0083540).